AMENDMENTS TO THE CLAIMS

1. (currently amended) A flash memory device comprising:

a plurality of sets of adjacent local bit lines;

a plurality of global bit lines; and

a plurality of select transistors each having a control gate, each select transistor is coupled between one of the local bit lines in each set of local bit lines and one of the global bit lines, wherein a first global bit line of the plurality of global bit lines is coupled to the select transistors of non-adjacent local bit lines ~~each local bit line in each set of local bit lines is coupled to a different global bit line~~.

2. (Original) The flash memory device of claim 1 further comprising:

a plurality of select lines to activate the control gates on the select transistors, each select line is coupled to the control gates on associated select transistors, wherein the associated select transistors are select transistors that are coupled to the local bit lines in an associated set of local bit lines.

3. (Original) The flash memory device of claim 1 wherein each set of local bit lines comprises two or more local bit lines.

4. (Original) The flash memory device of claim 1 wherein each set of local bit lines contains an even number of bit lines.

5. (canceled)

6. (currently amended) The flash memory device of claim [[5]] 1 further comprising:

a plurality of select lines to activate the control gates on the select transistors, each select line is coupled to the control gates on associated select transistors, wherein the associated select transistors are select transistors that are coupled to every other global bit line.

7. (currently amended) The flash memory device of claim [[5]] 1 wherein each set of local bit lines comprises four local bit lines.

8. (currently amended) The flash memory device of claim [[5]] 1 wherein the plurality of global bit lines comprises two global bit lines.

9-10 (canceled)

11. (currently amended) A flash memory device comprising:

a plurality of local bit lines positioned generally parallel with each other;

a plurality of select transistors, each transistor coupled to an associated one of the plurality of local bit lines; and

a plurality of global bit lines, each global bit line is coupled to a pair of associated select transistors, wherein the pair of select transistors are ~~coupled to~~ associated with alternate local bit lines.

12. (canceled)

13. (Original) The flash memory device of claim 11 wherein the device is manufactured so the local bit lines are on a different planer level than the global bit lines.

14. (canceled)

15. (currently amended) A flash memory system comprising:

an array of flash memory cells arranged in rows and columns;

a plurality of local bit lines positioned generally parallel with each other, each local bit line is coupled to an associated column of the memory array;

a plurality of global bit lines; and

a select circuit to selectively couple the local bit lines to the global bit lines, wherein a first global bit line of the plurality of global bit lines is coupled to non-adjacent local bit lines ~~every other local bit line is coupled to a different global bit line~~.

16. (Original) The flash memory system of claim 15 wherein the plurality of local bit lines comprise a first local bit line, a second local bit line, a third local bit and a fourth local bit line.

17. (Original) The flash memory system of claim 15 wherein the select circuit comprises a select transistor coupled to each of the plurality of bit lines.

18-37 (Cancelled)

38. (currently amended) A method of forming an integrated circuit comprising:

selectively coupling select transistors between a local bit line in a set of local bit lines and an associated global bit line, wherein each non-adjacent local bit line in the set of local bit lines is coupled to a first ~~different~~ global bit line; and

selectively coupling a select line to control gates of the select transistors coupled to the local bit lines in a set of local bit lines.

39. (Original) The method of claim 37, wherein each set of local bit lines contains an even number of bit lines.

40-54 (Cancelled)

55. (new) A flash memory device comprising:

a plurality of sets of adjacent local bit lines, each set comprising a first, second, third, and fourth local bit line;

a plurality of global bit lines including a first and a second global bit line; and

a plurality of select transistors each having a control gate, the plurality of select transistors are coupled between the plurality of sets of adjacent local bit lines and the plurality of global bit lines, wherein every other local bit line in one of the plurality of sets of local bit lines is coupled to a different one of the plurality of global bit lines such that the first global bit line is

coupled to the first and third local bit lines and the second global bit line is coupled to the second and fourth local bit lines.

56. (new) A flash memory device comprising:

a plurality of sets of adjacent local bit lines, each set comprising a first, second, third, and fourth local bit line;

a plurality of global bit lines including a first and a second global bit line;

a plurality of select transistors each having a control gate, the plurality of select transistors are coupled between the plurality of sets of adjacent local bit lines and the plurality of global bit lines, wherein the first global bit line is coupled to the first and third local bit lines and the second global bit line is coupled to the second and fourth local bit lines;

a first select line coupled to control gates of select transistors coupled to the first and second local bit lines; and

a second select line coupled to control gates of select transistors coupled to the third and fourth local bit lines.

57. (new) A flash memory device comprising:

a plurality of local bit lines positioned generally parallel with each other, the plurality of local bit lines include a first local bit line, a second local bit line, a third local bit and a fourth local bit line;

a plurality of select transistors coupled to an associated one of the plurality of local bit lines;

a plurality of global bit lines, each global bit line is coupled to a pair of associated select transistors, wherein the pair of select transistors are coupled to alternate local bit lines;

a first select line coupled to control gates of the select transistors coupled to the first and second local bit lines; and

a second select line coupled to control gates of the select transistors coupled to the third and fourth local bit lines.

58. (new) A flash memory device comprising:

a plurality of local bit lines positioned generally parallel with each other wherein the local bit lines are formed on a first metal level;

a plurality of select transistors coupled to an associated one of the plurality of local bit lines; and

a plurality of global bit lines, each global bit line is coupled to a pair of associated select transistors, wherein the pair of select transistors are coupled to alternate local bit lines and the global bit lines are formed on a second metal level.

59. (new) A flash memory system comprising:

an array of flash memory cells arranged in rows and columns;

a plurality of local bit lines positioned generally parallel with each other, each local bit line is coupled to an associated column of the memory array;

a plurality of global bit lines; and

a select circuit to selectively couple the local bit lines to the global bit lines, wherein every other local bit line is coupled to a different global bit line, the select circuit comprising a first select line to activate select transistors that are coupled to the first and second local bit lines and a second select line to activate select transistors that are coupled to the third and fourth local bit lines.